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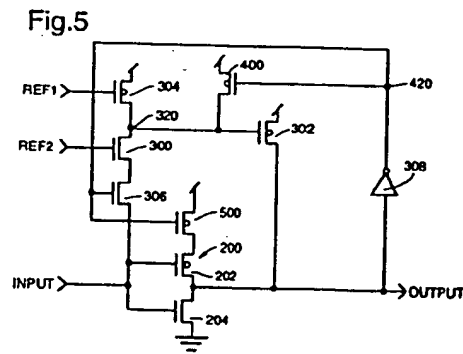
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(54) Input buffer utilizing a cascode.

(57) An input buffer for utilization in a programmable logic device (PLD). The input buffer includes an inverter (200) consisting of a PMOS pull up transistor (202) one half the size of a corresponding NMOS pull down transistor (204) to enable TTL compatibility. To drive a high capacitance load, instead of utilizing further buffering which introduces gate delays, a cascode transistor (300) is used to control an additional pull up output driver (302) connected to the output of the inverter (200). The cascode functions to turn on the additional pull up output driver (302) to supplement the PMOS pull up transistor (202) during a low to high transition of the output. The input buffer further includes a switching transistor (500) coupled between a V_{DD} power supply and the PMOS pull up transistor (202) to cut power to the PMOS pull up transistor (202) when the inverter (200) has a low output. With no utilization of power during a low output, the input buffer provides a zero power TTL input enabling the input buffer to be utilized on circuitry in battery powered devices.



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The present invention relates to an input buffer preferably of the type which provides an interface between a digital integrated circuit and circuitry external to the digital integrated circuit. Preferably, it relates to an input buffer for a programmable array logic (PAL) device.

Fig. 1 shows a block diagram for the AmPALCE22V10, a typical programmable logic device manufactured by Advanced Micro Devices, Inc. The internal circuitry of the AmPALCE22V10 is CMOS logic. To enable the circuitry of the AmPALCE22V10 to be compatible with circuitry external to the chip, which may be TTL logic, input buffers 100(a-1) are utilized.

The AmPALCE22V10 further includes output logic macrocells 102 connected to provide an output which registered or combinatorial. The output from the output logic macrocell can be fed back into an input buffer on the chip.

Fig. 2 shows typical prior art input buffer, such as that utilized on the AmPALCE22V10. In Fig. 2, an input signal to the input buffer is received by a CMOS inverter 200. In order for the input buffer of Fig. 2 to be TTL compatible, the CMOS inverter 200 should have a threshold at around 1.5 volts, assuming a valid TTL high level is 2.0 volts.

The 1.5 volt threshold is achieved by making the PMOS transistor 202 of inverter 100 relatively weak, or about half the size of the NMOS transistor 204. Note that circles on transistors, such as transistor 202, indicate a P-type transistor, while no circle on a transistor indicates an N-type transistor. With transistor 202 being half the size of transistor 204 inverter 200 has approximately a quarter of the drive capability because of the reduced mobility of holes in relation to electrons.

Note that a TTL high to a standard CMOS input will result in the PMOS 202 not turning off completely so that the first inverter will draw power. Typically, the input would have to be raised to within less than 1.0 volt of the supply voltage for the input stage to not draw power.

To avoid TTL high power consumption, extra steps may be added to a standard CMOS fabrication process to create a PMOS transistor which turns completely off at TTL high input levels.

Inverters 206 and 208 are added to the output of inverter 200 in order to drive a high capacitance node connected to the input buffer output. Note, however, that each inverter added to the signal path of the input buffer has an inherent gate delay so that the decision to add buffering in order to achieve the highest performance is dependent upon the capacitance level of circuitry connected to the output node of the input buffer.

The embodiment of the present invention to be described provides fewer gate delays than the input buffer of Fig. 2 to drive a capacitive load. Additionally,

it enables the input buffer to burn zero power with TTL high input level, enabling the input buffer to be utilized on circuitry in battery powered devices such as lap top computers.

It also allows compatibility to CMOS circuitry operating at different voltage levels such as between 5.0 volt CMOS, and 3.0 volt CMOS.

We will describe an input buffer circuit utilizing an inverter consisting of a PMOS pull up transistor one half the size of a corresponding NMOS pull down transistor to enable TTL compatibility as well as compatibility to lower voltage CMOS circuits. To drive a high capacitance load, instead of utilizing further buffering, a cascode transistor controls an additional pull up output driver connected to the output of the inverter. The cascode functions to turn on the additional pull up output driver to supplement the PMOS pull up transistor during a high to low transition of the input.

The input buffer utilizes feedback from the inverter output to control whether or not the source of the cascode is connected to the inverter input. In one embodiment, feedback is also utilized to provide an additional current source to more rapidly switch the output driver transistor off after the output has switched high.

In another embodiment, the input buffer of the present invention further includes a switching transistor coupled between a V_{DD} power supply and the PMOS pull up transistor to cut power to the PMOS pull up transistor when the input buffer has a high input. With no utilization of power during a high input, the input buffer provides a zero power TTL input enabling the input buffer to be utilized on circuitry in battery powered devices such as lap top computers.

BRIEF DESCRIPTION OF THE DRAWINGS

Further details of the present invention are explained with the help of the attached drawings in which:

Fig. 1 shows a block diagram for the AmPALCE22V10;

Fig. 2 shows a typical prior art input buffer;

Fig. 3 shows an embodiment of an input buffer of the present invention;

Fig. 4 shows the embodiment of Fig. 3 further utilizing an additional current source transistor connected to turn off the output driver transistor more quickly;

Fig. 5 shows the embodiment of Fig. 4 further utilizing a power supply switching transistor connected in series with the PMOS pull up transistor cutting power utilized to zero when the input buffer output is low;

Fig. 6 shows the non-zero power embodiment of Fig. 4 further utilizing circuitry to provide an inverted and a noninverted input buffer output; and Fig. 7 shows the embodiment of Fig. 6 with fur-

ther features added so that the input buffer may be utilized on the AmPALCE22V10.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 3 shows an embodiment of an input buffer of the present invention. As in Fig. 2, the input buffer of Fig. 3 includes an inverter 200 receiving an input data signal, the inverter including a PMOS pull up transistor 202 and an NMOS pull down transistor 204. As in Fig. 2, transistor 202 is approximately half the size of the transistor 204. For convenience, like reference numbers for components in the circuitry of Fig. 2 which are referenced in Fig. 3 are carried over.

Fig. 3 further includes a cascode amplifier 300 and a strong pull up driver transistor 302 which is configured to augment the relatively weak PMOS pull up transistor 202. A current source transistor 304 is connected to supply power to the cascode 300 and the gate of pull up driver transistor 302 at node 320. A weak current is supplied by current source transistor 304 as controlled by voltage reference REF1 applied to its gate. The weak current source is necessary so as not to load the input excessively during high to low transitions where the current sourced by transistor 304 must be overcome by whatever is driving the input.

A voltage reference REF2 is supplied to the gate of cascode 300 so that cascode 300 turns on when its source drops to somewhere in the vicinity of the desired input threshold, the threshold being 1.5 volts for TTL compatible inputs. A switching transistor 306 connects the source of cascode 300 to the input of inverter 200. An inverter 308 connected to the output of inverter 200 is connected to the gate of switching transistor 306 to control switching.

Note that a cascode transistor is a transistor defined by being turned on and off by varying voltage applied to the source with the gate voltage fixed, rather than varying the gate voltage. In a cascode transistor with $(V_g - V_s) > V_t$, wherein V_g is the gate voltage, V_s is the source voltage, and V_t is the threshold voltage of the transistor, the cascode transistor will turn on. With $(V_g - V_s) < V_t$, the cascode transistor will turn off.

In operation, when the input of Fig. 3 is low, NMOS pull down transistor 204 is off while PMOS pull up transistor 202 is on, thus pulling the output high. The output of inverter 308 will be low, thus turning off switching transistor 306. Because transistor 306 is off, the source of cascode 300 will be pulled up by current source 304 until cascode 300 turns off, approximately 1 volt below REF2. Node 320 will then be pulled up to V_{DD} , turning off pull up driver transistor 302. At this point, the only transistor holding the output high is PMOS pull up transistor 202.

When the input goes high, 3 volts for instance, NMOS transistor 204 turns on overcoming PMOS

transistor 202. Note that with 3 volts on its gate, PMOS transistor 202 does not turn off, but does source significantly less current which is overcome by NMOS transistor 204 to pull down the output. When the output is low, inverter 308 turns on switching transistor 306. At this point nothing happens, for as long as the input is high, cascode 300 remains off.

When the input goes low, NMOS transistor 204 turns off and PMOS transistor 202 turns on more strongly. Simultaneously, cascode 300 turns on overcoming current source 304 to pull node 320 low which turns on pull up driver transistor 302. Pull up driver transistor 302 and PMOS pull up transistor 202 together pull up the output. Pull up driver transistor 302 supplies sufficient current so that no further buffering is required for connecting the input buffer output to a substantial capacitive load.

When the output goes high again, inverter 308 turns off transistor 306 and operation continues as described above.

Fig. 4 shows the embodiment of Fig. 3 further utilizing an additional transistor 400 connected to turn off the output driver transistor 302 more quickly. Transistor 400 has a gate connected to the output of inverter 308 at node 420. The drain of current source transistor 400 is connected to supply power from V_{DD} to node 320 to which the gate of output driver transistor 302 is connected. For convenience, like reference numbers are utilized for components in the circuitry of Fig. 4 which are carried over from Fig. 3.

In operation, when node 420 goes low after a low to high transition of the output, current source transistor 400 will turn on to more rapidly pull node 320 high in order to turn output driver transistor 302 off more quickly.

Fig. 5 shows the embodiment of Fig. 4 further utilizing a power supply switching transistor 500 connected between the V_{DD} power supply and the PMOS pull up transistor 202. The gate of power supply switching transistor 500 is connected to inverter 308 to be controlled by the input buffer output. For convenience, like reference numbers are utilized for components in the circuitry of Fig. 5 which are carried over from Fig. 4.

In operation, when the input buffer input is at a TTL high, the input buffer output will be low turning off power supply switching transistor 500 to cut off the supply of current to PMOS pull up transistor 202. Switching transistor 500, thus, enables zero power operation.

When the input buffer input goes low, the low to high transition of the output is now handled exclusively by pull up driver transistor 302 because PMOS pull up transistor 202 will be disabled by switching transistor 500. Cascode 300 turns on which pulls down node 320 and turns on pull up driver transistor 302 which pulls up the output.

When the output is high, inverter 308 pulls node

420 low which turns off switching transistor 306, thus isolating the cascode 300. The inverter 308 additionally turns the additional current source transistor 400 on which assists current source 304 in pulling node 320 high to turn off pull up driver transistor 302. The inverter further turns on power supply switching transistor 500 which enables PMOS transistor 202 to hold the output high.

When the input goes high again, operation continues as described above.

Fig. 6 shows the non-zero power embodiment of Fig. 4 further utilizing circuitry to provide an inverted and a noninverted input buffer output. For convenience, like reference numbers are utilized for components in the circuitry of Fig. 6 which are carried over from Fig. 4.

The input of Fig. 6 is connected to the inverter 200 as well as an additional inverter 600 containing an PMOS pull up transistor 602 and an NMOS pull down transistor 604. The output of inverter 200 supplies the inverting output, while inverter 600 is connected at node 652 directly to the gates of inverter transistors 626 and 628 as well as directly to inverter transistor 622 and indirectly to inverter transistor 624 to control the supply of power to the noninverting output.

Node 652 is connected indirectly to the gate of transistor 624 through node 654 by transistor 616. Node 654 further supplies an inverter 630 connected to the gate of transistor 632 which connects the inverting output to ground. Node 654 is tied to node 652 when the noninverted output is low by transistor 634 which has its gate connected to the noninverting output.

The output of inverter 200 is connected through an inverter 308 to a node 420 similar to Fig. 4. In addition to driving switching transistor 306 as in Fig. 4, node 420 also drives switching transistor 606 connecting node 652 to the gate of inverter transistor 622. Additionally, in Fig. 6, node 420 is connected by an inverter 608 to node 650. Transistor 610 has a gate connected to provide hysteresis feedback from node 650 provides to control node 420.

Node 650 provides a gate input to a current source transistor 614, an NMOS version of PMOS current source transistor 400 of Fig. 4. Current source transistor 614 provides supplemental current to pull up driver transistor 302 for inverter 200 as well as for a pull up driver transistor 612 for inverter 600. Node 650 further provides a gate input to inverter transistors 616 and 618 as well as a switching transistor 620 connecting the gate of inverter transistor 622 to ground.

In operation, we assume initially that the input is low making the inverted output high by means of PMOS pull up transistor 202. With the inverting output high, inverter 308 will provide a low to node 420 which turns off switching transistors 306 and 606 allowing node 320 to be pulled high. Inverter 608 will output a

high with transistor 610 adding hysteresis which turns on transistors 614, 616 and 620. Transistor 616 being on allows current to flow in the gate of transistor 624. By means of PMOS pull up transistor 602 of inverter 600, node 652 is pulled high which turns off transistor 626, turns on transistor 628, and by virtue of the fact that transistor 616 is on, turns transistor 624 off bringing the noninverting output low.

When the input is brought high, NMOS pull down transistor 204 turns on and overcomes PMOS transistor 202 and thus begins to pull down the inverted output. Likewise, NMOS pull down transistor 604 turns on and overcomes PMOS transistor 602. Node 652 will have much less capacitance than the inverted output so that it will be pulled down more quickly. Because transistor 616 is on, node 654 via inverter 630 turns on transistor 632 to assist NMOS transistor 204 in pulling down the inverted output. Because nodes 652 and 654 are both low, transistors 624 and 626 will be on and transistor 628 will turn off thus bringing the non-inverting output high. After the inverting output goes low, inverter 308 pulls up node 420 which turns on transistors 306 and 606. Inverter 608 then pulls down node 650 which turns off transistors 614, 620, and 616 while turning on transistor 618. Transistors 624 and 632 are thus disabled, while transistor 622 is enabled.

When the output is brought low, cascode 300 turns on pulling node 320 low. Node 320 had been pre-charged to .7 volts below the V_{DD} supply voltage by transistors 304 and 636. With node 320 low, driver transistor 302 and 612 turn on assisting PMOS transistors 202 and 602 in pulling up the inverted output and node 652 respectively. When node 652 is pulled high, transistors 622 and 628 are turned on while transistor 626 is turned off, thus pulling down the non-inverting output. Inverter 308 then pulls node 420 low which turns off transistors 306 and 606. Inverter 608 then pulls node 650 high which turns on transistor 614 to pull up node 320 to $V_{DD}-1$ volt. Transistor 620 is turned on which turns off transistor 622.

Fig. 7 shows the embodiment of Fig. 6 with further features added so that the input buffer may be utilized on the AmpALCE22V10. Fig. 7 utilizes the circuitry of Fig. 6 along with additional circuitry for providing a registered feedback input and circuitry for providing an edit mode. For convenience, like reference numbers are utilized for components in the circuitry of Fig. 7 which are carried over from Fig. 6.

Registered feedback is provided at the QBF input of transistor 700 of Fig. 7, while normal inputs are provided at the I/O input of transistor 702. AC1HV and AC1HVB are input signals provided to the gates of transistors 702 and 700 respectively to enable either the I/O input or the QBF input respectively. Transistors 700 and 702 are connected to provide an output to the input buffer circuitry at node 720 which makes up the input of the input buffer of Fig. 6. Note that the

letter "B" in input labels, such as in QBF and AC1HVB, indicate these inputs are active low, while "HV" indicates a high voltage is applied.

In operation with registered feedback, I/O is chosen as the input with AC1HV high and AC1HVB low. Registered feedback is provided when AC1HVB is high and AC1HV is low. Registered feedback is provided from the output macrocell as shown in Fig. 1. During edit mode, AC1HV and AC1HVB are both low to isolate the input node 720.

An edit mode is provided by transistor 704, 706 and 708 receiving an EDT gate input and a transistor 710 receiving an EDTHVB gate input. Transistor 704 is connected between the V_{DD} and PMOS pull up transistor 200 similar to transistor 500 of Fig. 5 enabling a zero power consumption. Transistor 706 connects the input to ground and transistor 708 connects the input of transistor 606 at node 703 to ground. Transistors 710 connects node 652 and transistor 606.

In operation with an edit mode, EDTHVB is low which turns off transistor 710. EDT is high which turns off transistor 704 disabling PMOS transistor 202 and turns on transistors 706 and 708 which pull down nodes 720 and 730 respectively. Nodes 720 and 730 being low turn off transistor 628 and transistors 204 and 604 respectively an turns on transistor 602 Transistor 602 pulls up node 652 to turn off transistor 626. REF2 is low which turns off cascode 300 allowing current source 304 to pull up node 320 and turn off driver transistor 302. Node 650 is in an unknown state depending upon whether the inverting output is high or low.

If node 650 is high, then node 652 will pull up node 654 through transistor 616 thus turning off transistor 624 and transistor 632 via inverter 630. Note that transistor 624 is latched to node 652 if the non-inverting output is low via transistor 634. Transistor 620 will then pull node 740 low turning off driver transistor 612.

If node 650 is low then transistor 618 will be on, again pulling up node 654. Node 420 will be high which will turn on transistor 606 tying node 740 to node 730 which is already low. Thus, both the inverting and noninverting outputs are tristated.

Although the invention has been described above with particularity, this was merely to teach one of ordinary skill in the art how to make and use the invention. Many modifications will fall within the scope of the invention, as that scope as defined by the following claims.

Claims

1. An input buffer comprising:
 - an inverter having an inverter input and an inverter output;
 - a current source;

- a pull up driver transistor connected to supply power to the inverter output, the pull up driver transistor having a gate coupled to the current source; and
 - a cascode transistor coupled to the gate of the pull up driver transistor and to the current source to control a supply of current from the current source.

2. The input buffer of claim 1 wherein the inverter comprises:
 - a pull up transistor; and
 - a pull down transistor which supplies substantially more current than the pull up transistor.

3. The input buffer of claim 1 wherein the inverter comprises:
 - a pull up transistor with a threshold voltage which is TTL compatible; and
 - a pull down transistor.

4. The input buffer of claim 1 further comprising:
 - a switching transistor coupling a source of the cascode transistor to the inverter input, the switching transistor having a gate coupled to the inverter output.

5. The input buffer of claim 1 further comprising:
 - a supplemental current source having a gate coupled to the inverter output, the supplemental current source coupled to supply current to the gate of the pull up driver transistor.

6. The input buffer of claim 1 further comprising:
 - an inverter power supply; and
 - a zero power switching transistor having a current path coupled between the inverter power supply and the inverter, the zero power switching transistor having a gate coupled to the inverter.

7. A method of operating an input buffer comprising:
 - receiving power from a power supply;
 - receiving an input data signal, the input data signal having a buffer turn on state and a buffer turn off state;
 - utilizing substantially no power during the buffer turn off state of the input data signal; and
 - utilizing power from the power supply during the buffer turn on state of the input data signal to supply an output signal.

8. The method of claim 7 wherein the input data signal is a TTL compatible signal.

9. An input buffer for a programmable array logic device, the programmable array logic device having a PAL input for receiving either a registered input or a nonregistered input, the input buffer compris-

ing:

an inverter having an inverter input for receiving the PAL input and an inverter output for supplying a buffer output, the inverter comprising:

a pull up transistor; and
a pull down transistor substantially larger than the pull up transistor;
a current source transistor;
a pull up driver transistor connected to supply power to the inverter output, the pull up driver transistor having a gate coupled to the current source transistor;
a cascode transistor having a drain coupled to the gate of the pull up driver transistor and to the current source transistor; and
a switching transistor coupling a source of the cascode transistor to the inverter input, the switching transistor having a gate coupled to the inverter output.

10. The input buffer of claim 9 further comprising:
a supplemental current source having a gate coupled to the inverter output, the supplemental current source coupled to supply current to the gate of the pull up driver transistor.
11. The input buffer of claim 9 further comprising:
an inverter power supply; and
a zero power switching transistor having a current path coupled between the inverter power supply and the pull up transistor of the inverter, the zero power switching transistor having a gate coupled to the inverter output.

Fig.1. (1/2)
PRIOR ART

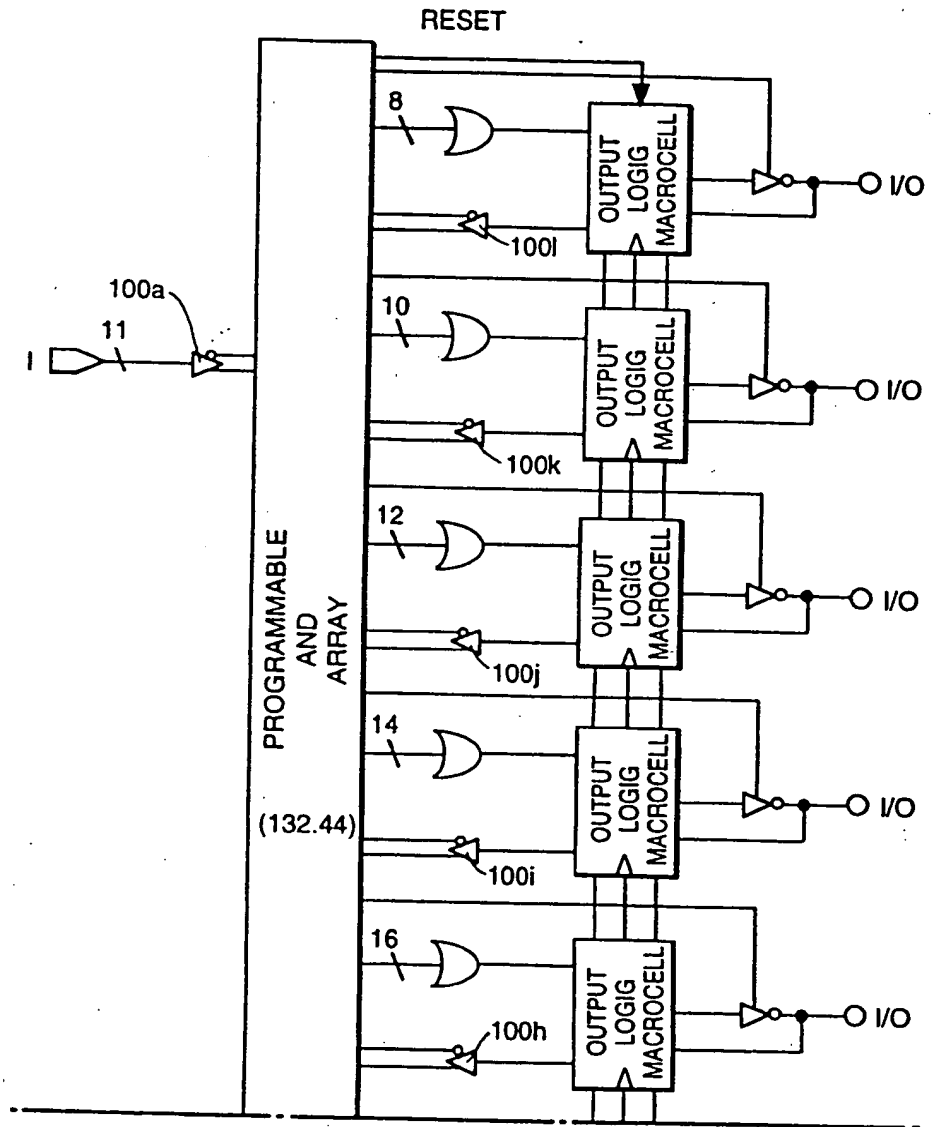


Fig.1. (2/2)

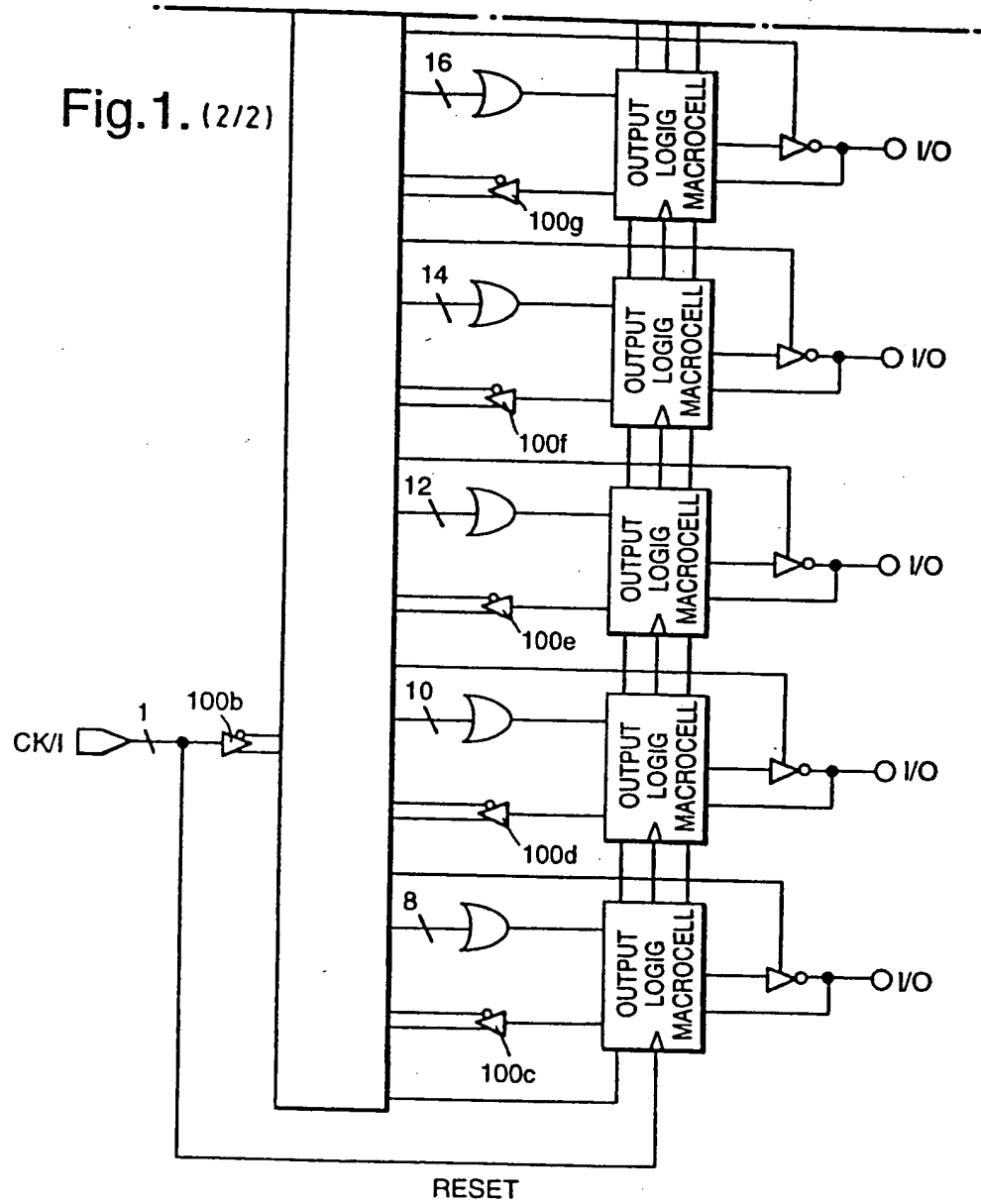


Fig.2
PRIOR ART

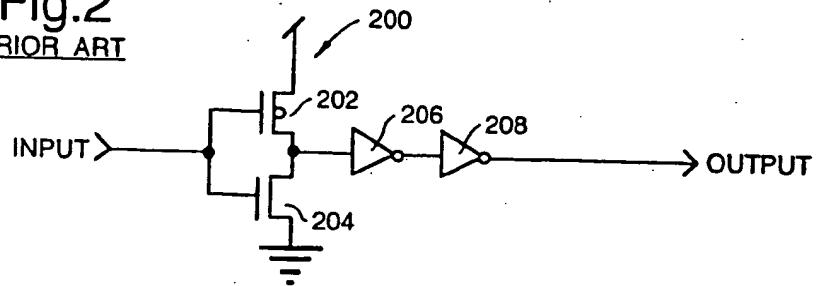


Fig.3

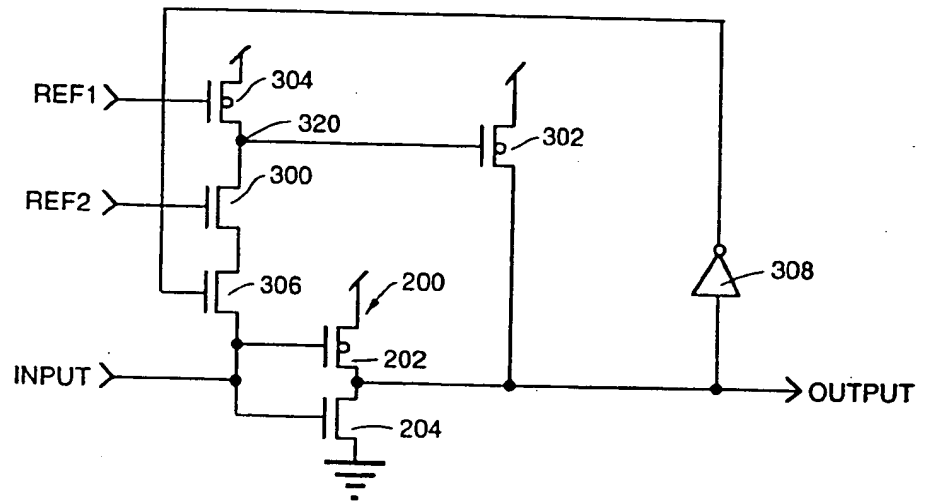


Fig.4

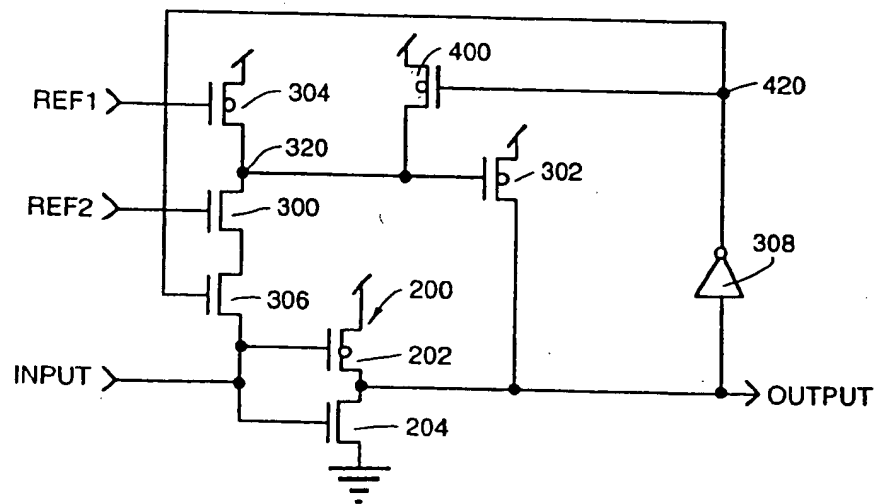
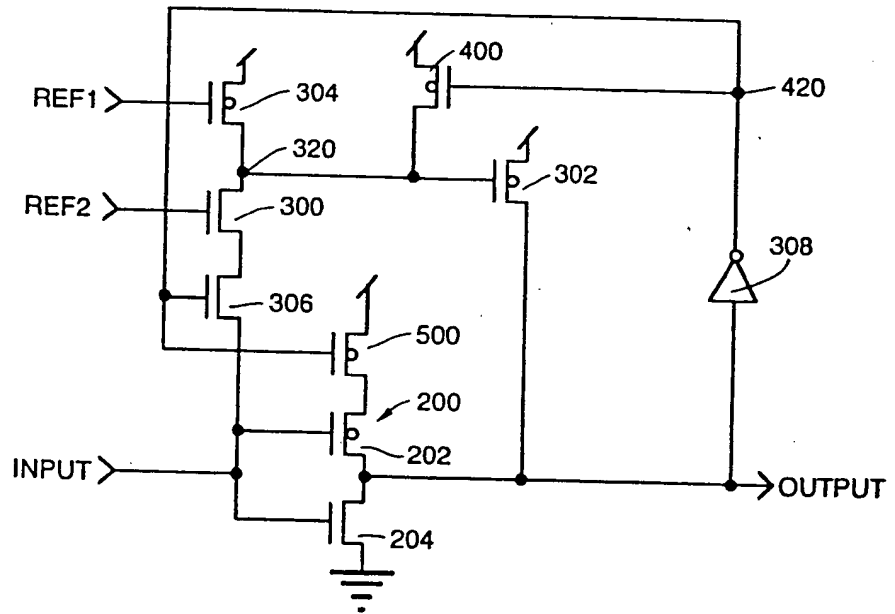


Fig.5



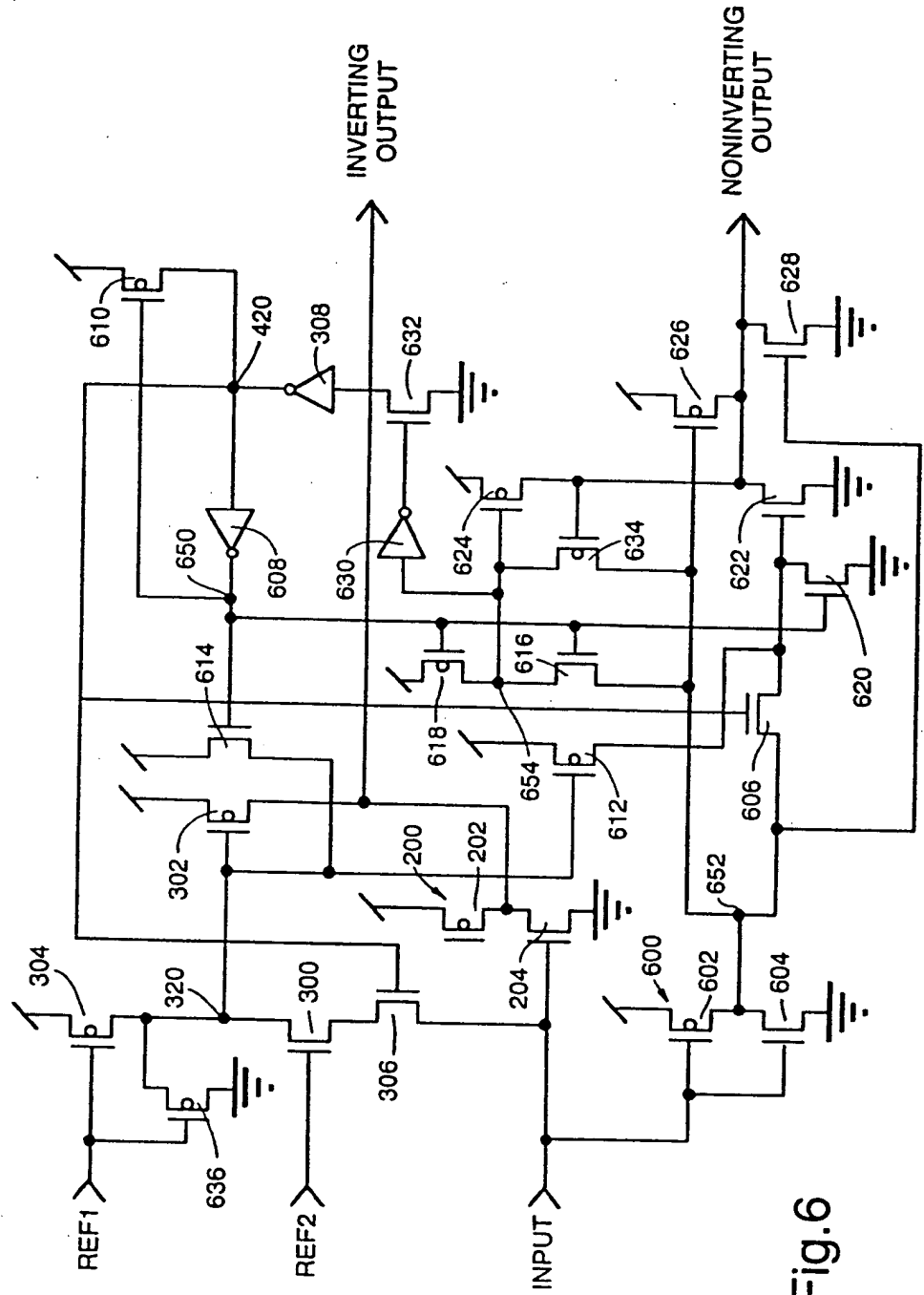
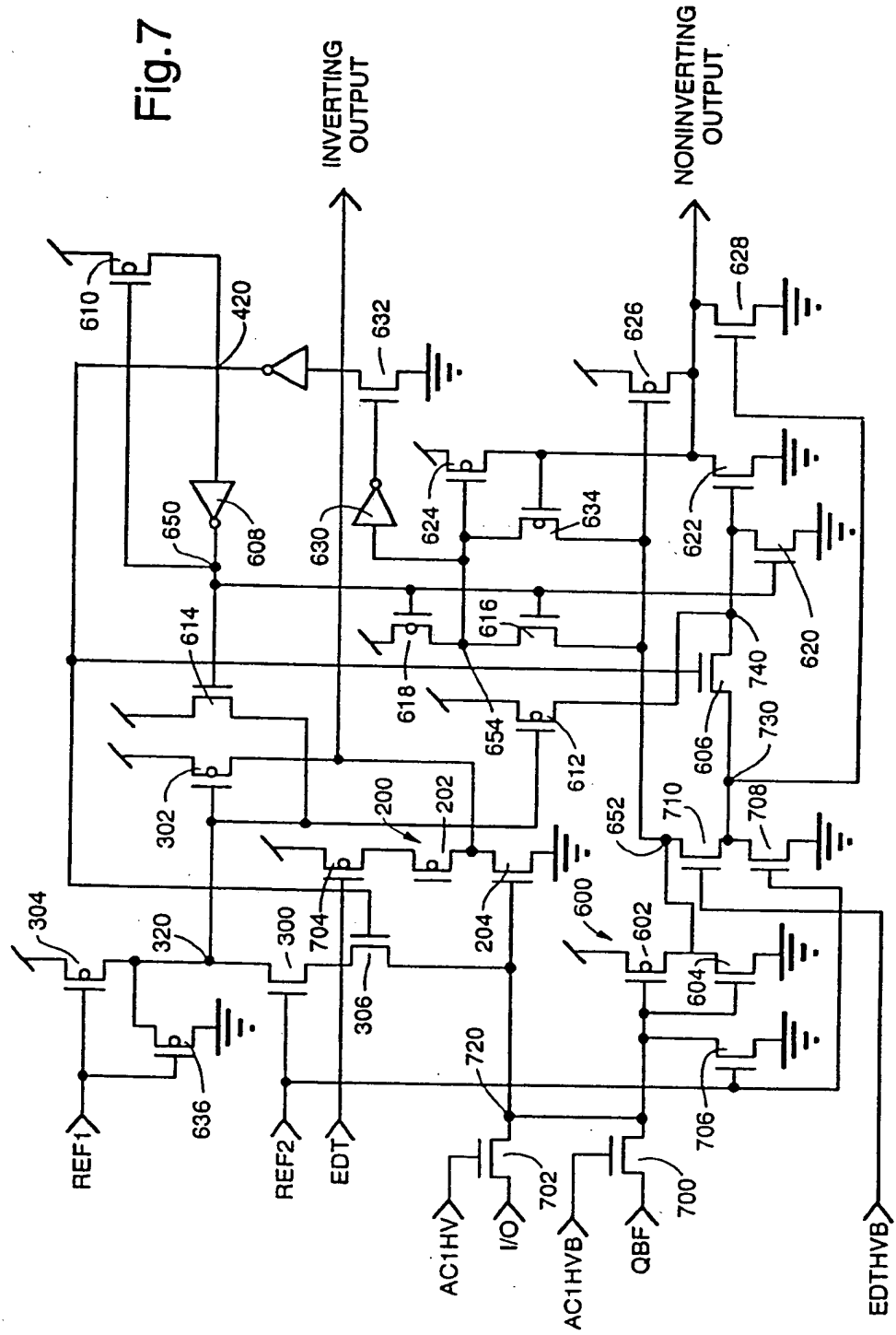


Fig.6

Fig.7





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 1299

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. CL.5)
A	US-A-4 593 212 (Y. SVAGER) *abstract; figure* * column 1, line 58 - column 4, line 4 *	1-3	H03K19/017 H03K19/0185 H03K19/00
A	US-A-5 144 167 (C. MC CLINTOCK) * abstract; figure 1 *	1-3,7	
X	PATENT ABSTRACTS OF JAPAN vol. 11, no. 306 (E-546) (2753) 6 October 1987 & JP-A-62 098 911 (SEIKO EPSON CORP) 8 May 1987 * abstract *	7,8	
X	US-A-4 825 106 (D. G. TIPON ET AL.) * abstract; claim 1; figure 3 * * column 3, line 10 - line 24 *	7	
A	US-A-4 672 243 (H. C. KIRSCH) * abstract; figure 3 *	7	
A	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol.23, no.4, August 1988, NEW YORK, NY, US pages 916 - 922 S. E. WAHLSTROM ET AL.: 'An 11000-Fuse Electrically Erasable Programmable Logic Device (EEPLD) with an Extended Macrocell' * figure 1 *	9	TECHNICAL FIELDS SEARCHED (Int. CL.5) H03K
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 6 July 1994	Searcher Arendt, M
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